

FIG. 1A

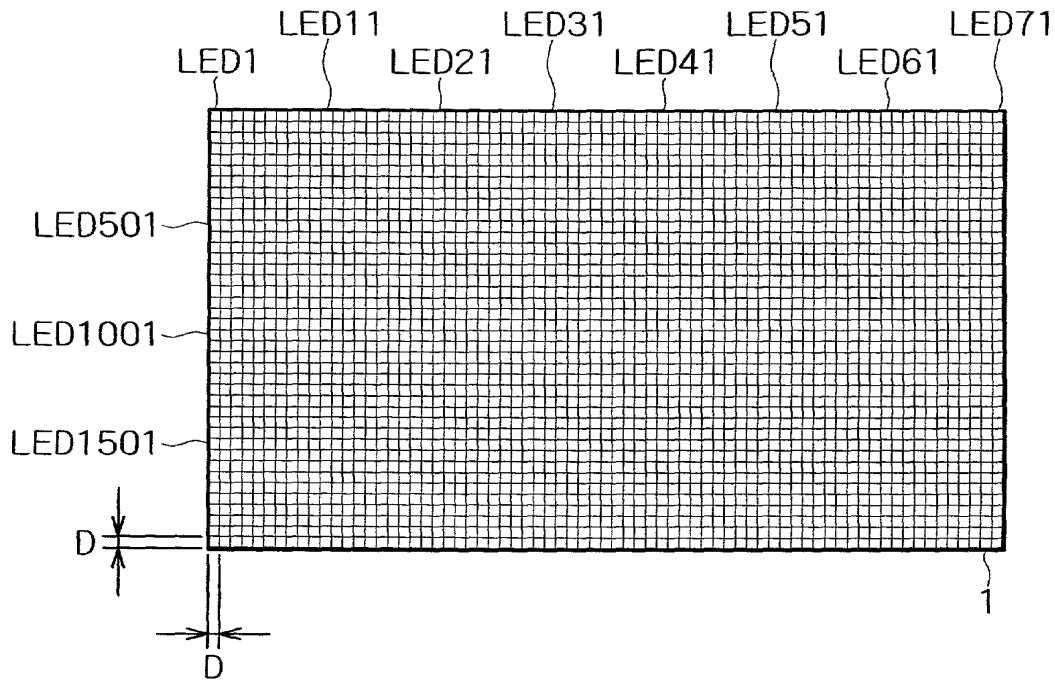


FIG. 1B

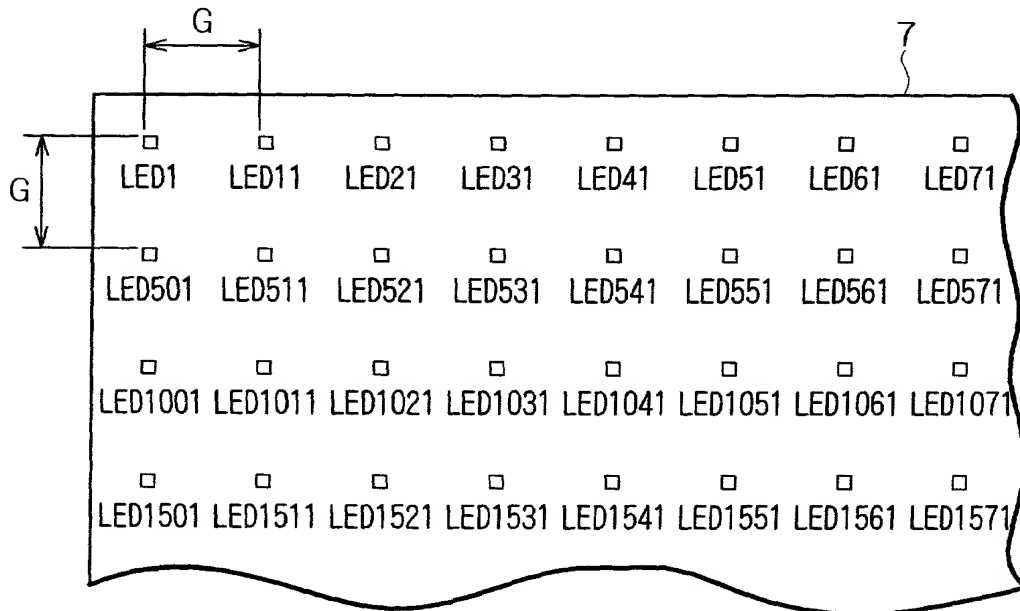
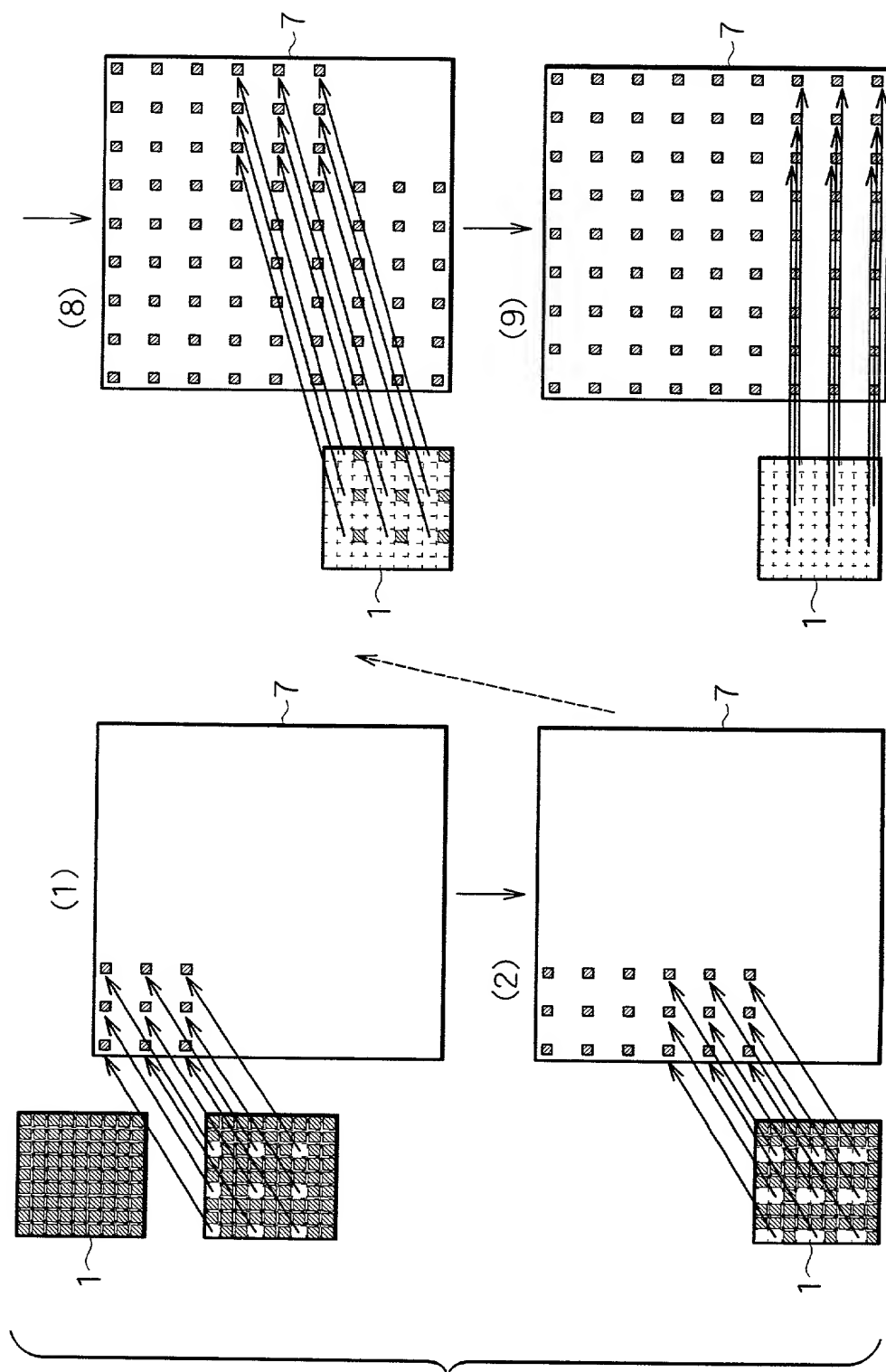


FIG. 2



3
G.
—
F

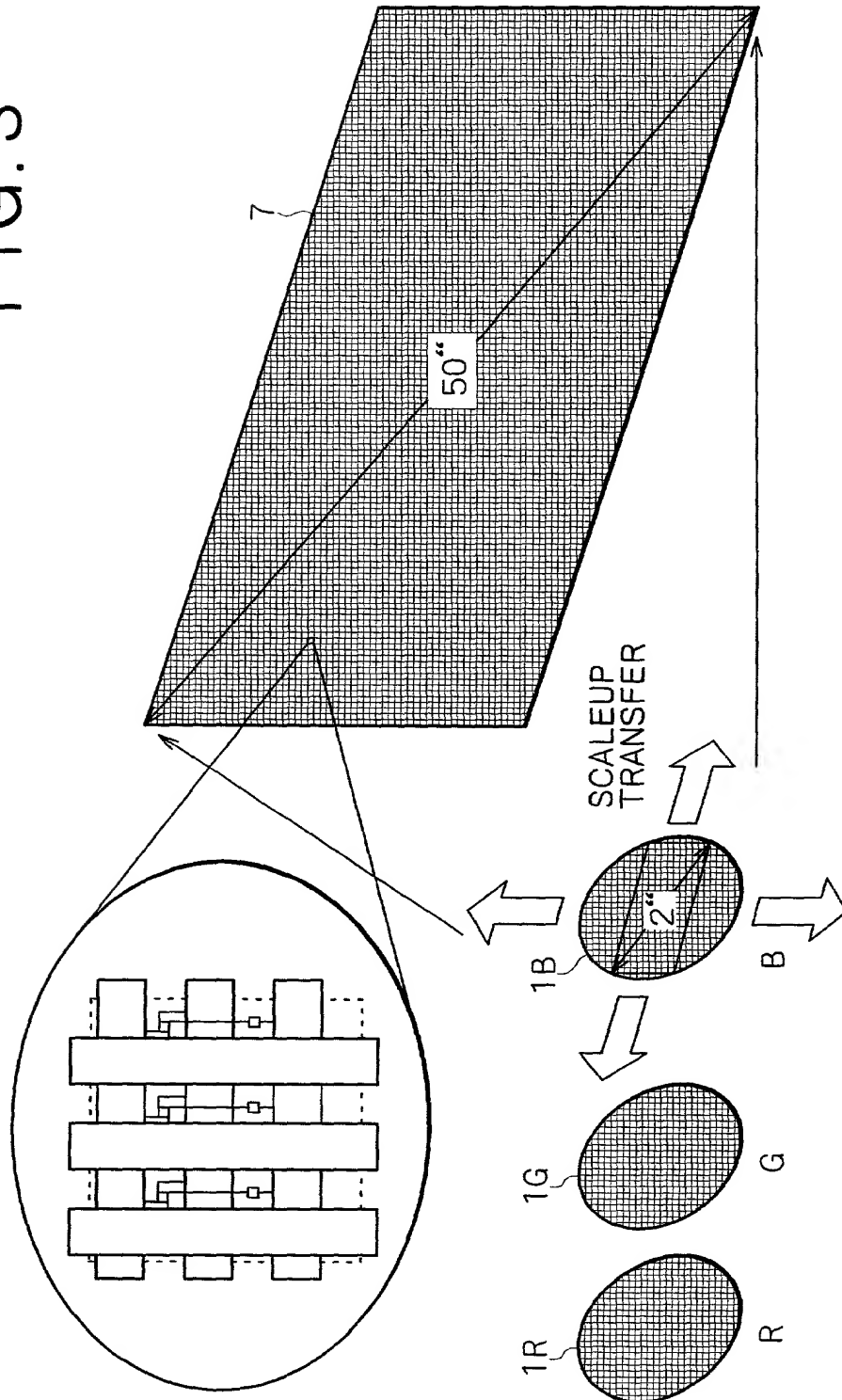


FIG. 4

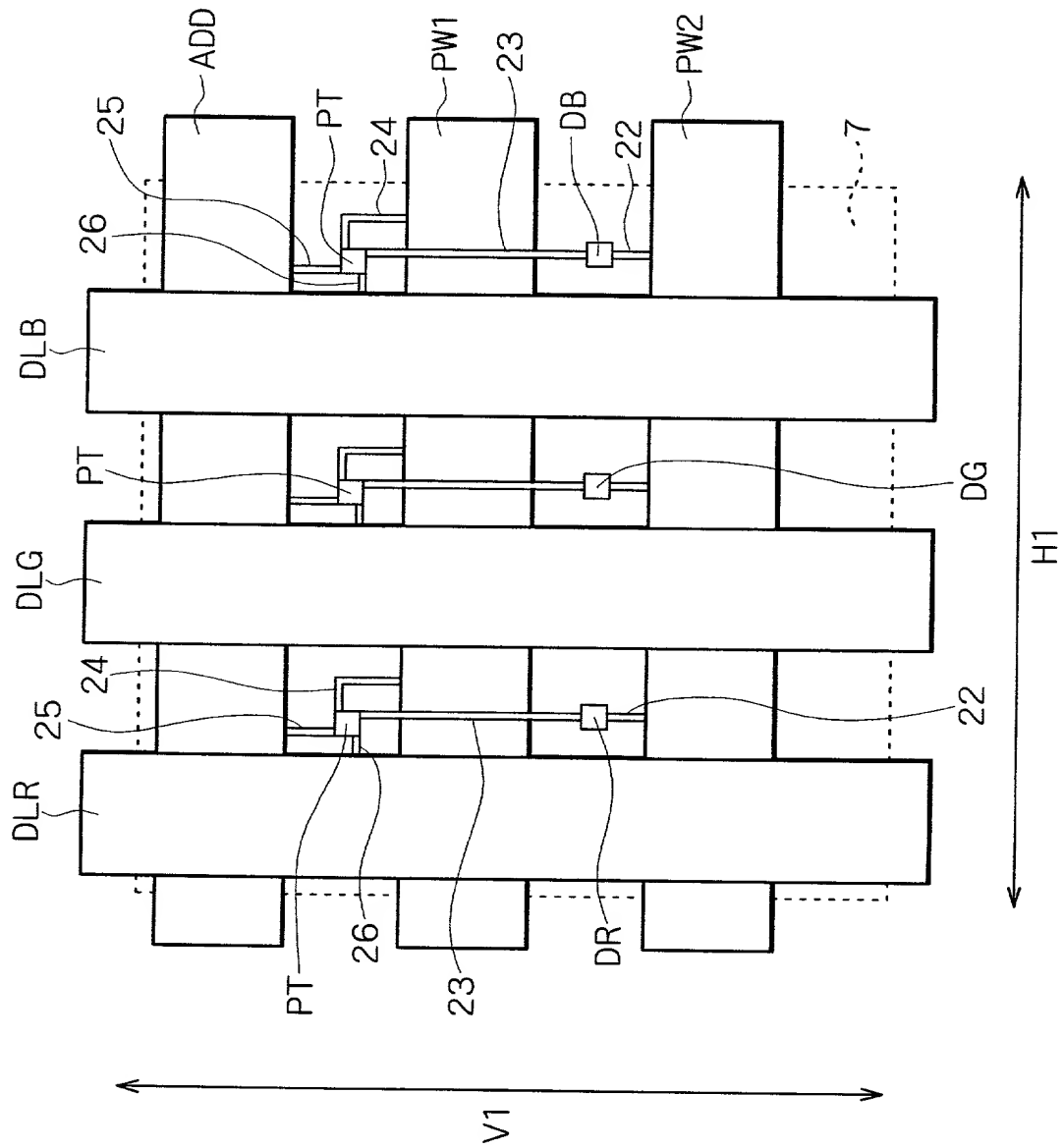


FIG. 5 is a schematic diagram of a video signal processing circuit. The circuit includes a shift register/gate (35) and a shift register (36). The shift register/gate (35) receives an image signal and horizontal synchronization signals. The shift register (36) receives vertical synchronization signals. The circuit is configured to process the image signal and synchronization signals to generate an output signal.

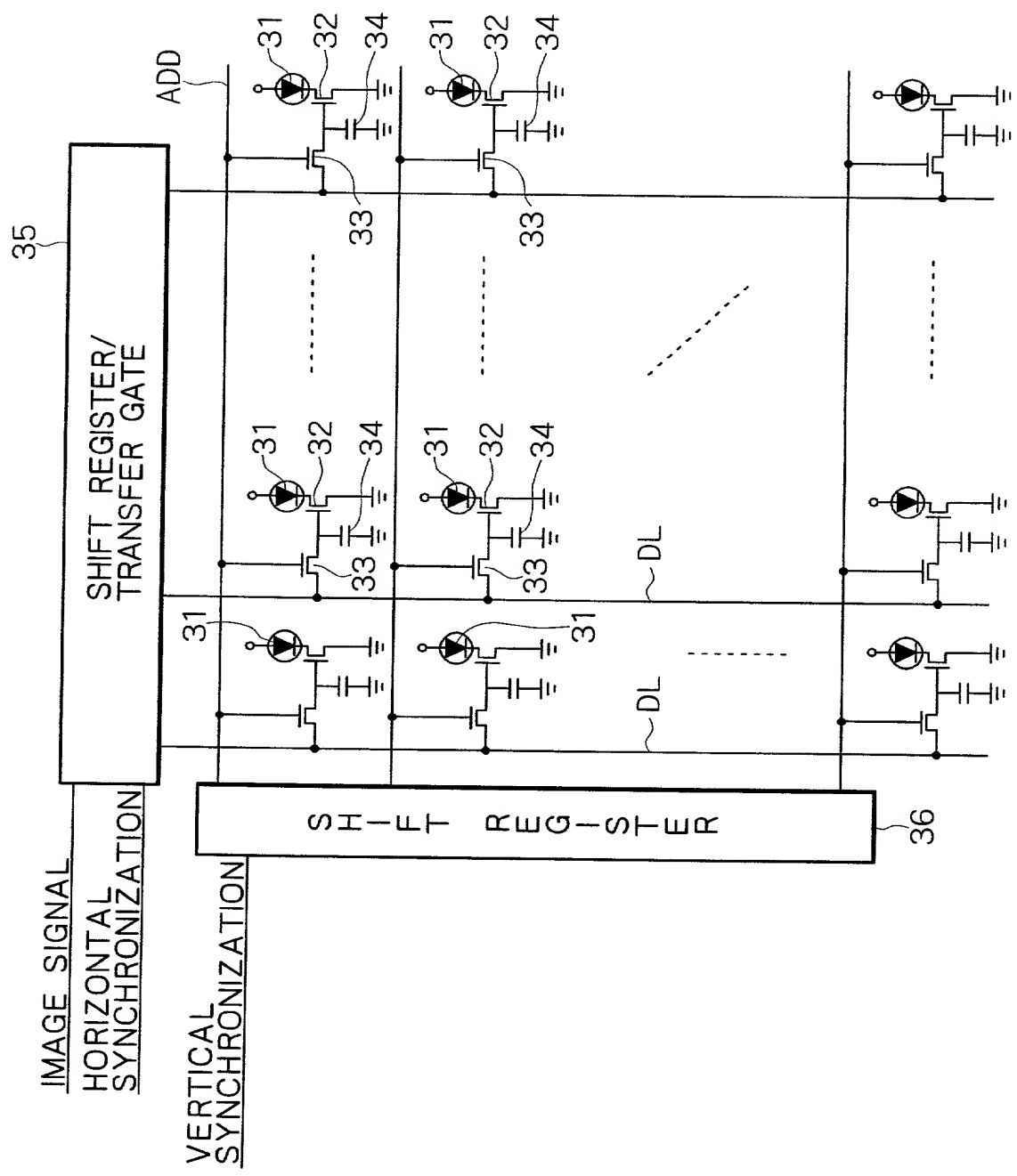


FIG. 5

FIG. 6A

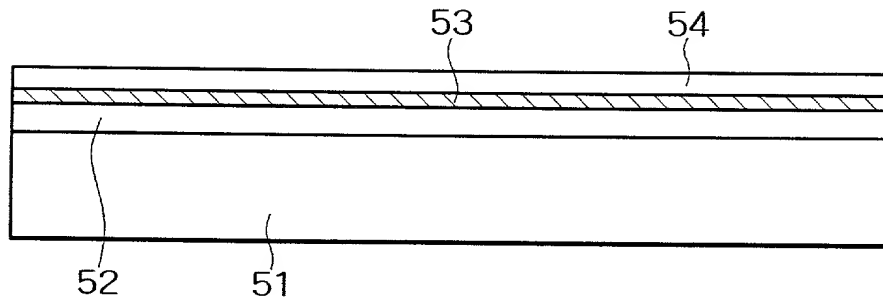


FIG. 6B

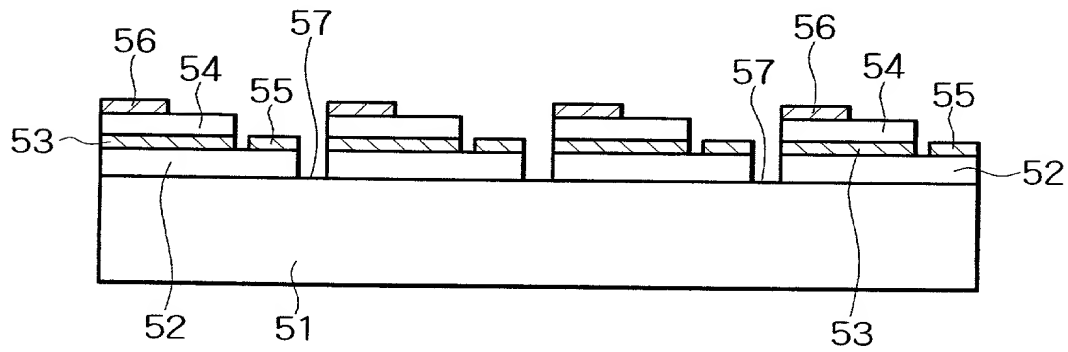


FIG. 6C

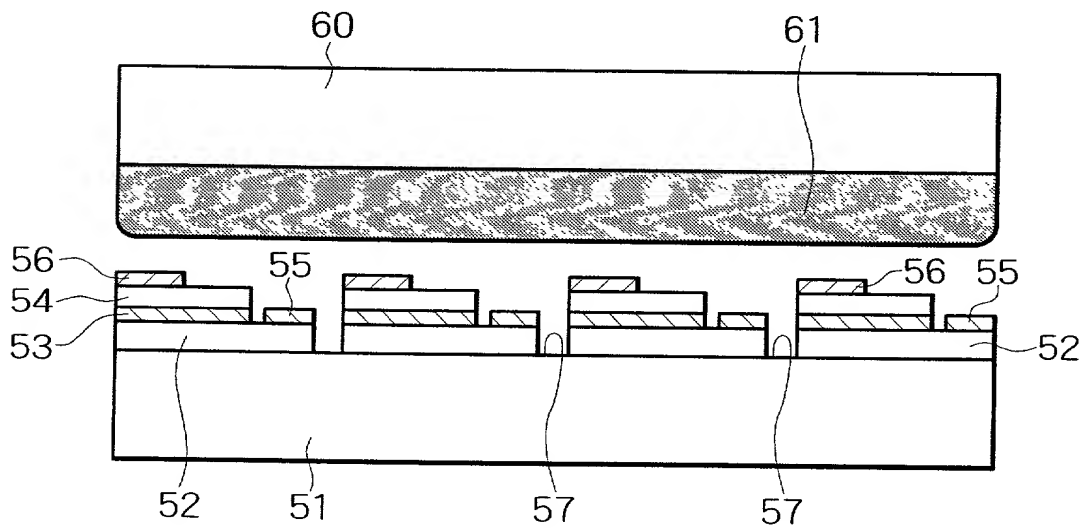


FIG. 6D

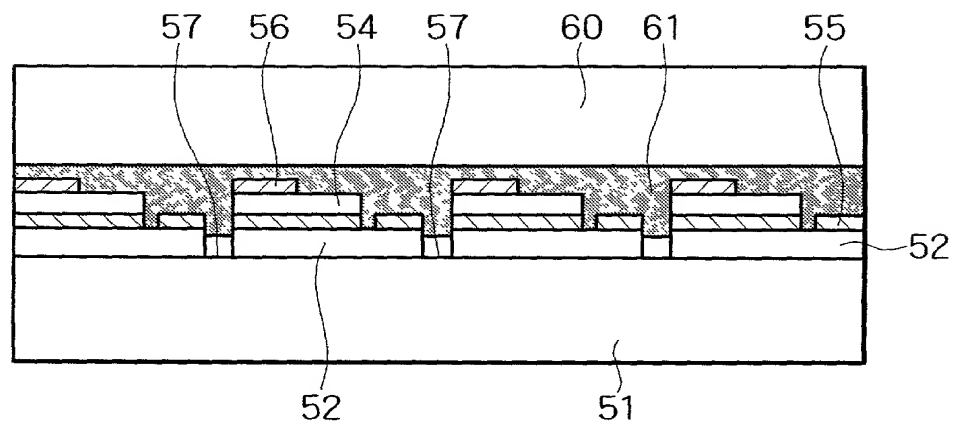


FIG. 6E

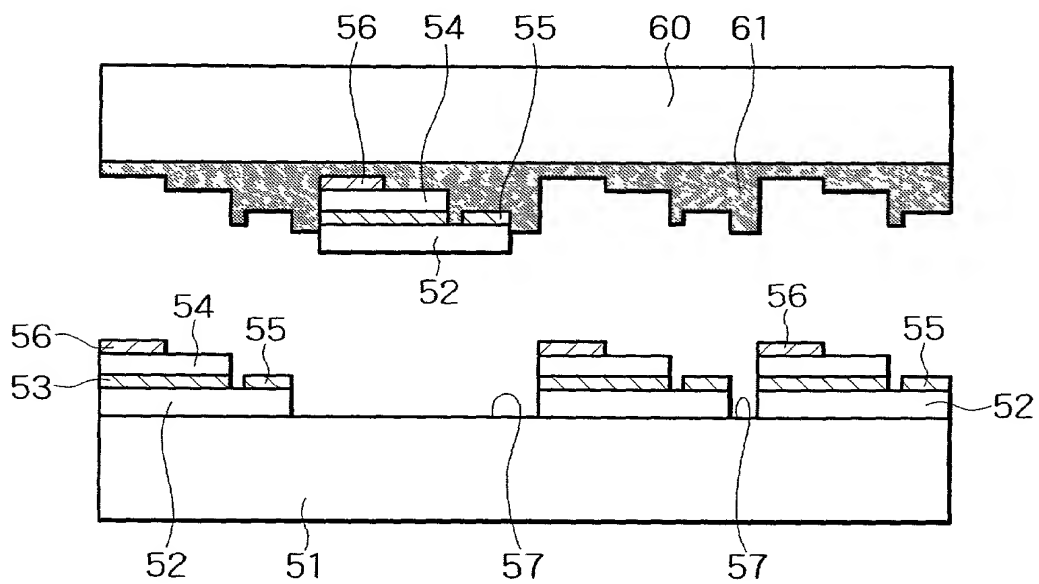


FIG. 6F

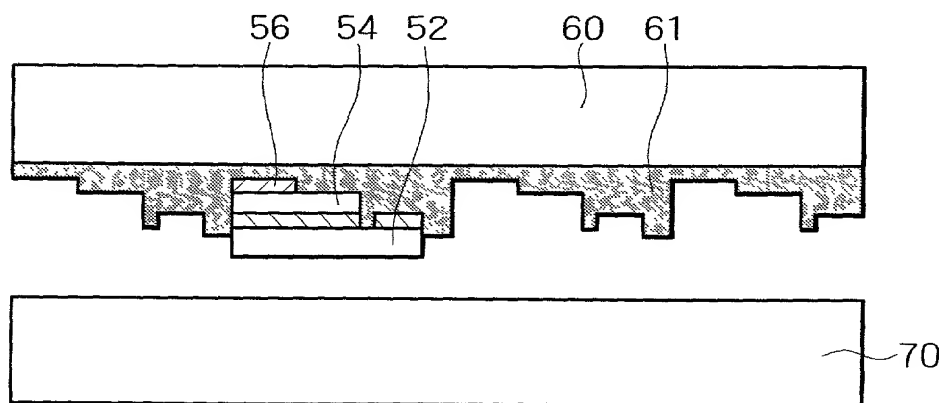


FIG. 6G

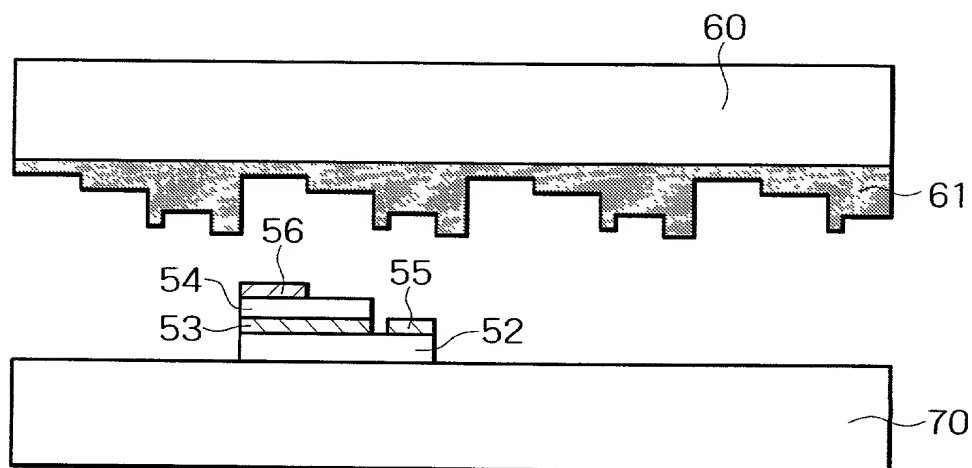


FIG. 6H

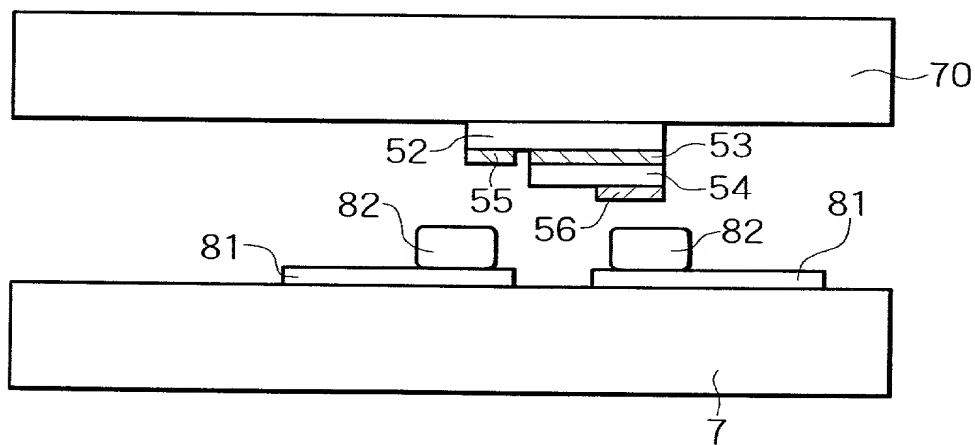


FIG. 6I

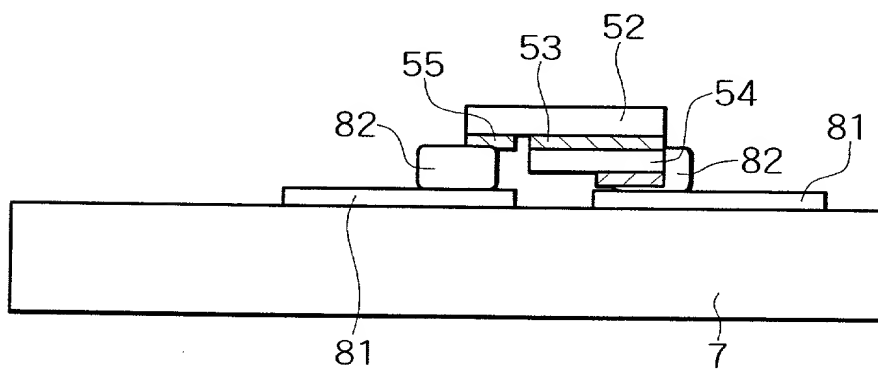


FIG. 7

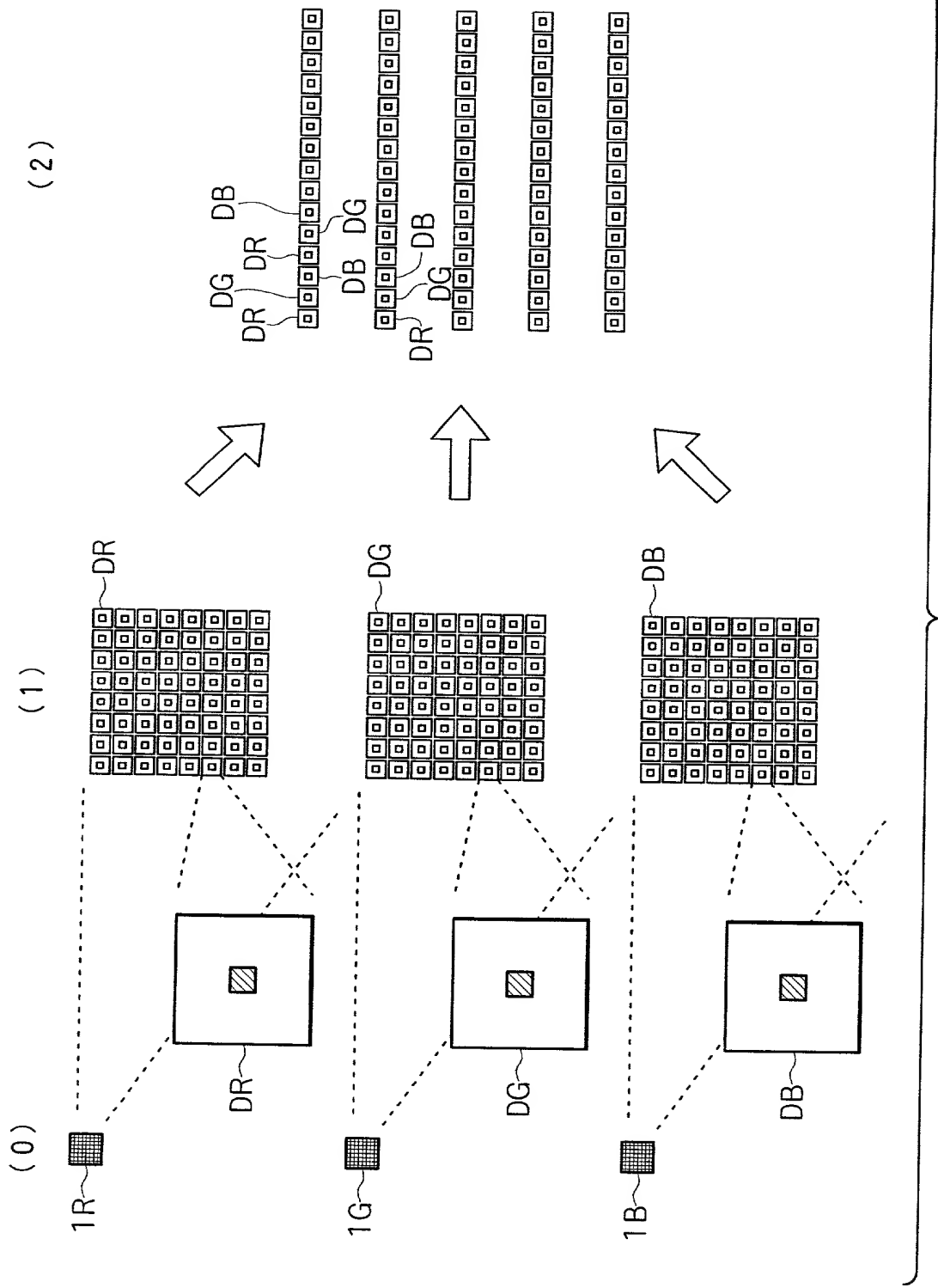


FIG. 8A

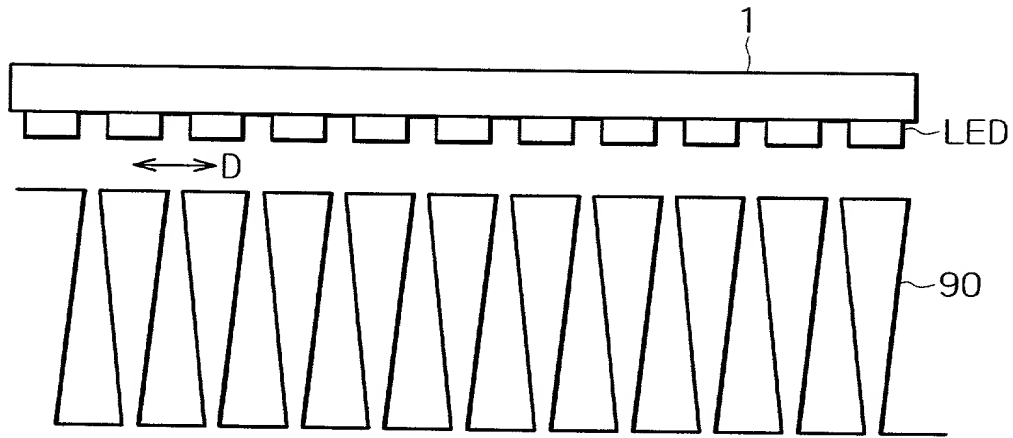


FIG. 8B

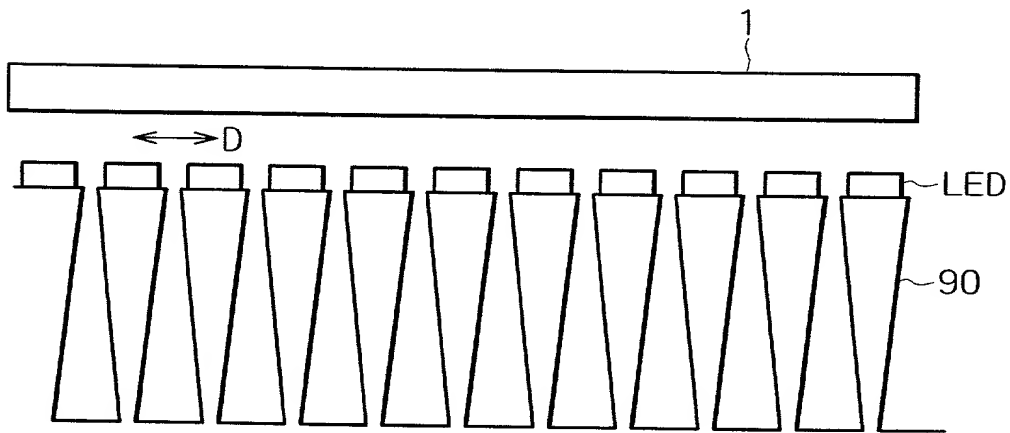


FIG. 8C

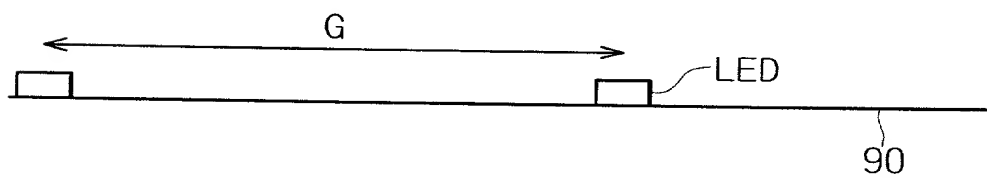


FIG. 9

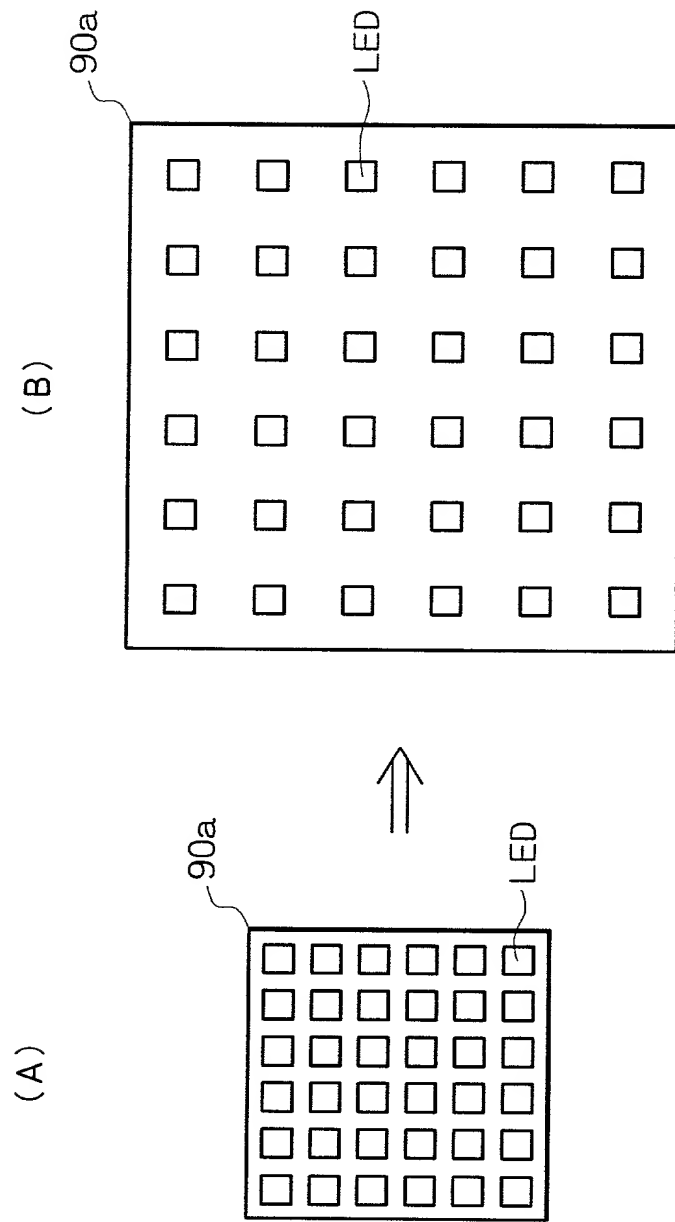


FIG. 10

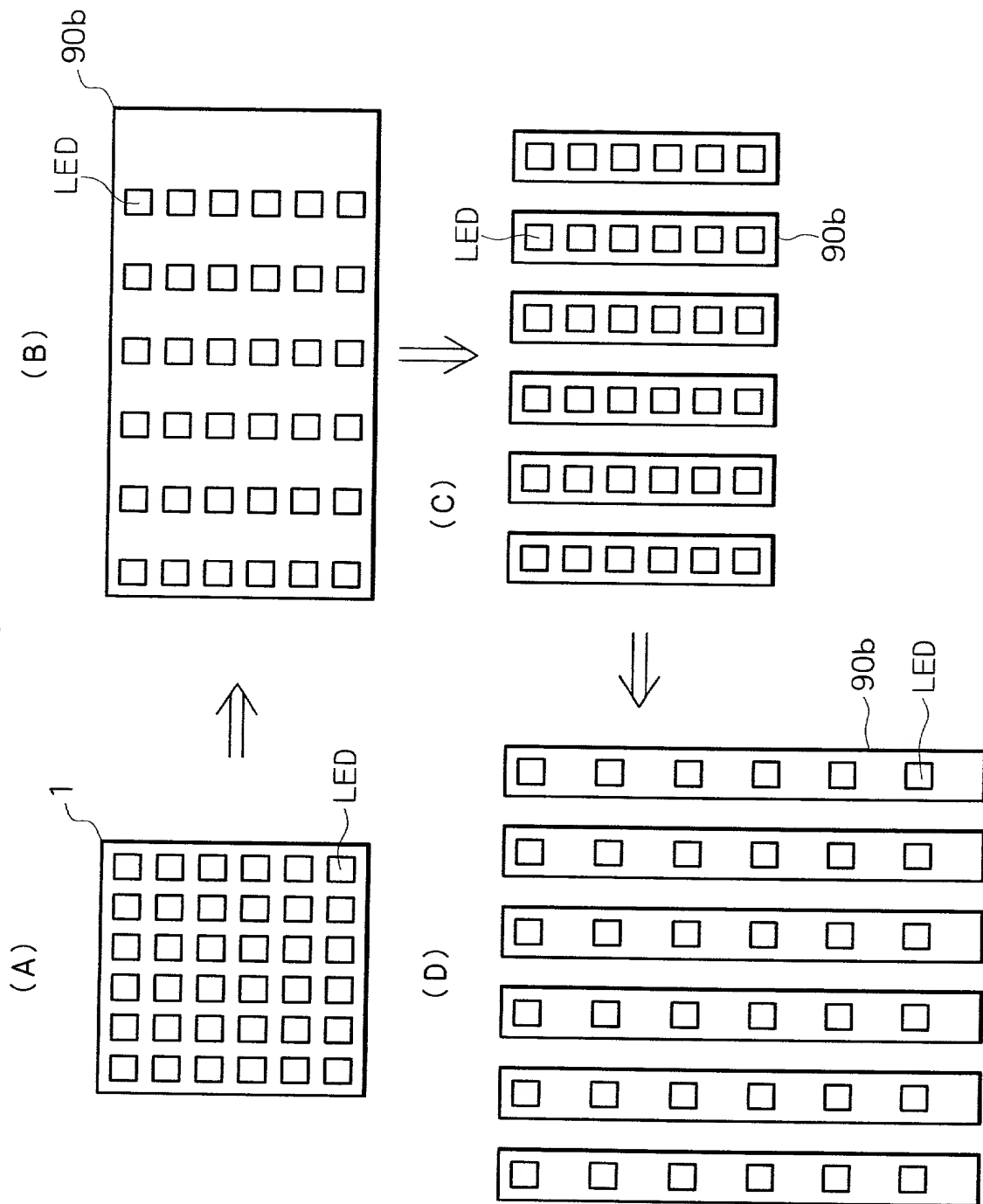


FIG. 11A

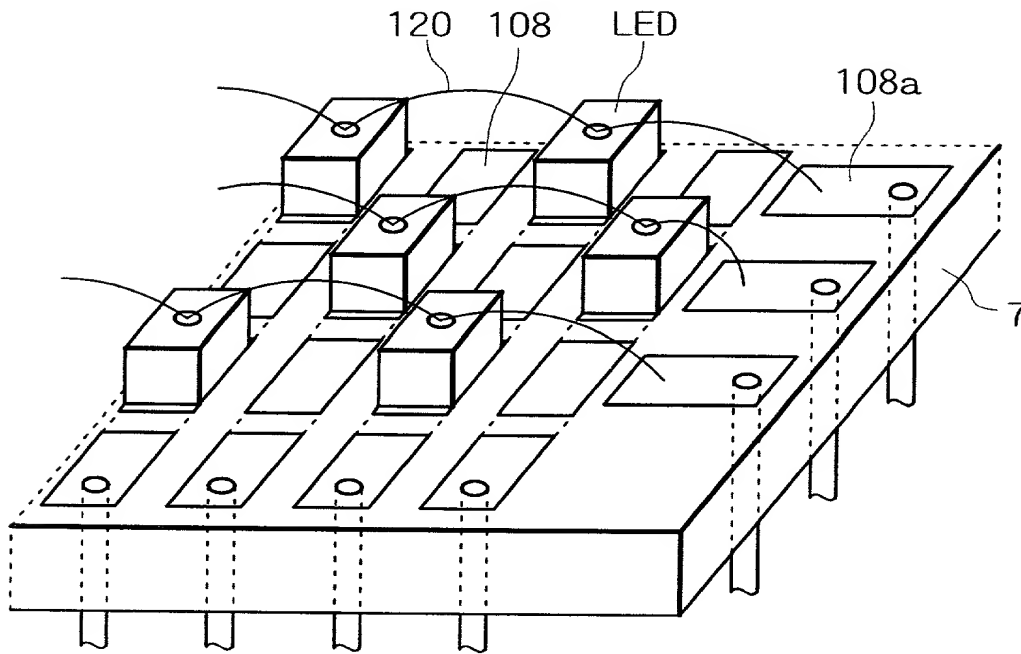


FIG. 11B

